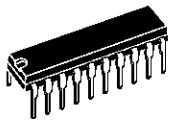
SGS-THOMSON MICROELECTRONICS

L6234

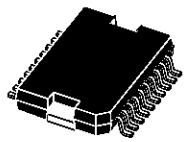
THREE PHASE MOTOR DRIVER

ADVANCE DATA

- SUPPLY VOLTAGE FROM 7 TO 52V
- 5A PEAK CURRENT
- $R_{DS\ ON}$ 0.3Ω TYP VALUE AT 25°C
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVER
- OPERATING FREQUENCY TO 50KHz
- THERMAL SHUTDOWN
- INTRINSIC FAST FREE WHEELING DIODES
- INPUT AND ENABLE FUNCTION FOR EVERY HALF BRIDGE
- 10V EXTERNAL REFERENCE AVAILABLE
- UNDERVOLTAGE LOCKOUT



POWER DIP (16+2+2)



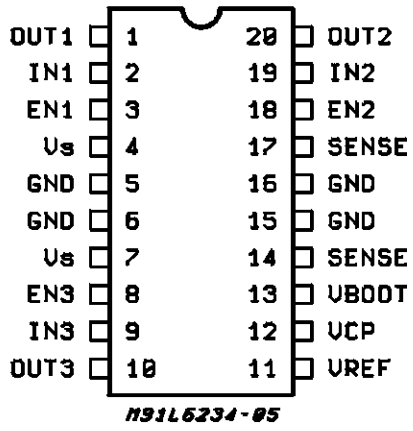
PowerSO20
(Jedec MO-166)

ORDERING NUMERS: L6234 (POWER DIP 16+2+2)
L6234PD (PowerSO20)

DESCRIPTION

The L6234 is a triple half bridge to drive a brushless motor.
It is realized in Multipower BCD technology wich combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip.
By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performances.
The output DMOS transistors can sustain a very high current due to the fact that the DMOS structure is not affected by the second breakdown effect, the maximum RMS maximum current is practically limited by the dissipation capabilies of the package. All the logic inputs are TTL, CMOS and µP compatible. Each channel is controlled by two separate logic input.
L6234 is available in 20 pin POWER DIP package (16+2+2) and in PowerSO20.

PIN CONNECTION (Top view)



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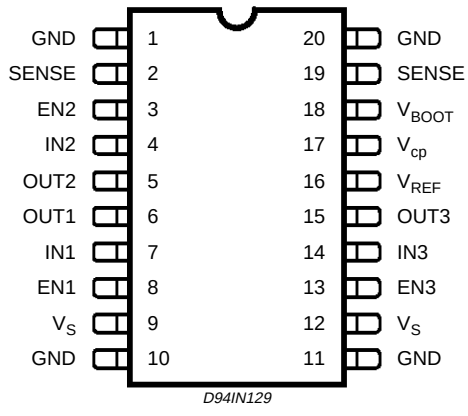
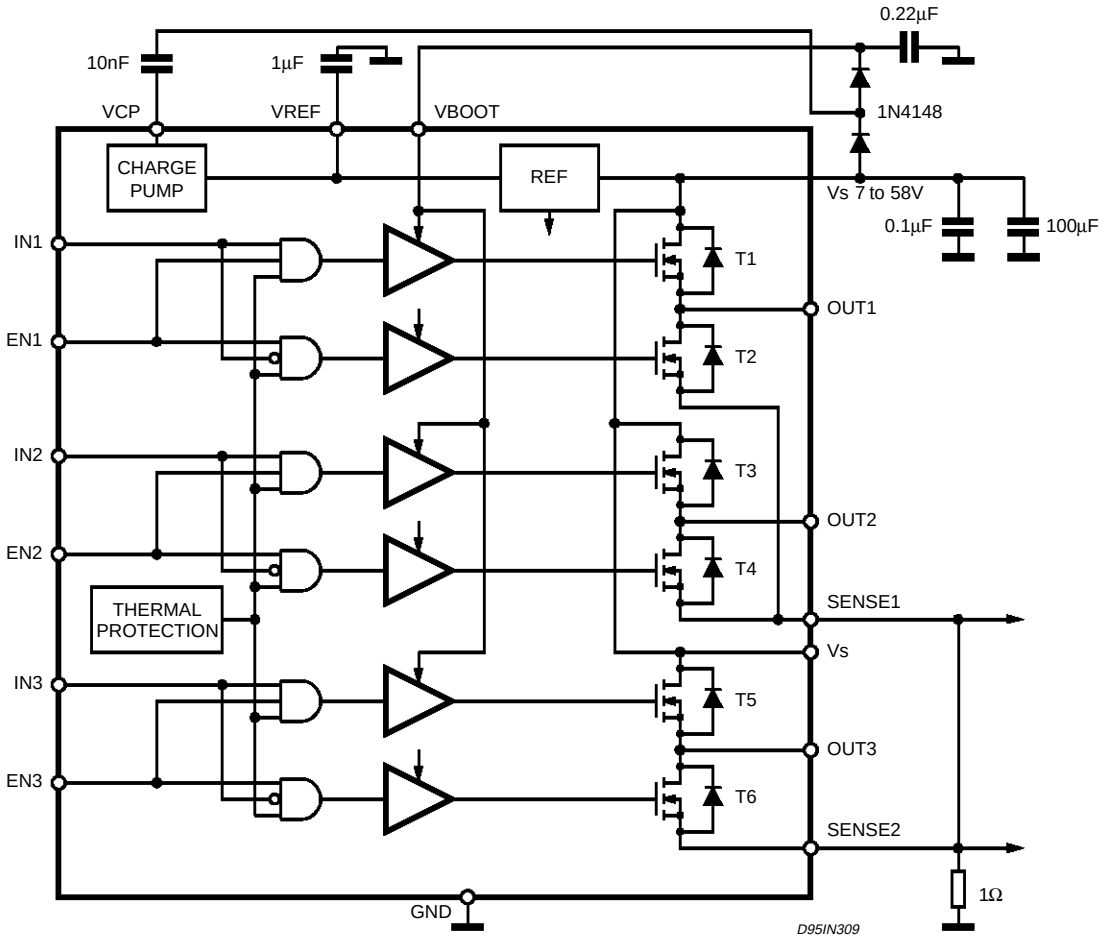
POWER DIP (16+2+2)



D94IN129

PowerSO20

BLOCK DIAGRAM



THERMAL DATA

Symbol	Parameter	DIP16+2+2	PowerSO20	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance, Junction to Pin	12	–	°C/W
$R_{th\ j\text{-}amb1}$	Thermal Resistance, Junction to Ambient (see Thermal Characteristics)	40	–	°C/W
$R_{th\ j\text{-}amb2}$	Thermal Resistance, Junction to Ambient (see Thermal Characteristics)	50	–	°C/W
$R_{th\ j\text{-}case}$	Thermal Residance Junction-case	–	1.5	°C/W

THERMAL CHARACTERISTICS

$R_{th\ j\text{-}pins}$

DIP16+2+2. The thermal resistance is referred to the thermal path from the dissipating region on the top surface of the silicon chip, to the points along the four central pins of the package, at a distance of 1.5 mm away from the stand-offs.

$R_{th\ j\text{-}amb1}$

If a dissipating surface, thick at least 35 µm, and with a surface similar or bigger than the one shown, is created making use of the printed circuit.
Such heatsinking surface is considered on the bottom side of an horizontal PCB (worst case).

$R_{th\ j\text{-}amb2}$

If the power dissipating pins (the four central ones), as well as the others, have a minimum thermal connection with the external world (very thin strips only) so that the dissipation takes place through still air and through the PCB itself.

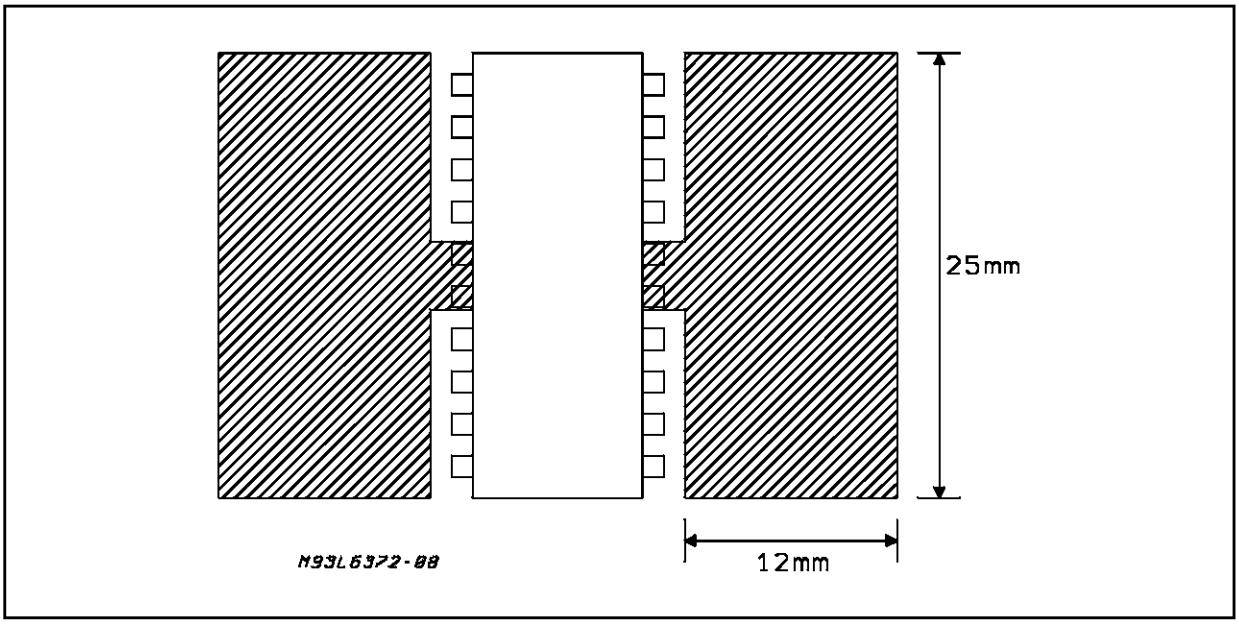
It is the same situation of point above, without any heatsinking surface created on purpose on the board.

Additional data on the PowerDip and the PowerSO20 package can be found in:

Application Note AN467:
Thermal Characteristics of the PowerDip 20,24 Packages Soldered on 1,2,3 oz. Copper PCB

Application Note AN668:
A New High Power IC Surface Mount Package: PowerSO20 Power IC Packaging from Insertion to Surface Mounting.

Figure 1: Printed Heatsink



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_P	Power Supply Voltage	58	V
V_{IN},V_{EN}	Input Enable Voltage	– 0.3 to 7	V
I_{peak}	Pulsed Output Current (note)	5	A
V_{SENSE}	Sensing Voltage	-1 to 4	V
V_b	Bootstrap Peak Voltage	68	V
V_{OD}	Differential Output Voltage (between any of the 3 OUT pins)	60	V
P_{tot}	Total Power Dissipation **L6234D** T_{pins} = 90°C	3.3	W
P_{tot}	Total Power Dissipation **L6234D** T_{amb} = 70°C	0.9 (*)	W
T_{stg}, T_j	Storage and Junction Temperature Range	-40 to 150	°C

Note 1: Pulse width limited only by junction temperature and the transient thermal impedance
(*) Mounted on board with minimized copper area

PIN FUNCTIONS

DIP/SO	PowerSO-20	Name	Function
1 20 10	6 5 15	OUT 1 OUT 2 OUT 3	Output of the channels 1/2/3.
2 19 9	7 4 14	IN 1 IN 2 IN 3	Logic input of channels 1/2/3. A logic HIGH level (when the corresponding EN pin is HIGH) switches ON the upper DMOS Power Transistor, while a logic LOW switches ON the corresponding low side DMOS Power.
3 18 8	8 3 13	EN 1 EN 2 EN 3	Enable of the channels 1/2/3. A logic LOW level on this pin switches off both power DMOS of the related channel.
4,7	9, 12	V_s	Power Supply Voltage.
14,17	2,19	SENSE	A resistance Rsense connected to this pin provides feedback for motor current control (the two pins must be connected together).
11	16	V_{ref}	Internal Voltage Reference. A capacitor connected from this pin to GND increases the stability of the Power DMOS drive circuit.
12	17	V_{cp}	Bootstrap Oscillator. Oscillator output for the external charge pump.
13	18	V_{BOOT}	Overvoltage input to drive the upper DMOS
5,6 15,16	1,10 11,20	GND	Common Ground Terminal. In Powerdip and SO packages these pins are used to dissipate the heat forward the PCB.

ELECTRICAL CHARACTERISTICS (V_S = 42V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		7		52	V
V_{ref}	Reference Voltage			10		V
I_S	Quiescent Supply Current			4		mA
f_C	Commutation Frequency				50	KHz
T_S	Thermal Shutdown		150			°C
T_D	Dead Time Protection			300		ns
V_h	Under Voltage Upper Threshold			6.5		V
V_l	Under Voltage Lower Threshold			6		V

OUTPUT DMOS TRANSISTOR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{DSS}	Leakage Current				1	mA
$R_{DS\ (ON)}$	ON Resistance			0.3		Ω
V_{sense}	Sensing Voltage		-1		4	V

SOURCE DRAIN DIODE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SD}	Forward ON Voltage	I_{SD} = 1.2A; EN = LOW		0.9		V
T_{RR}	Reverse Recovery Time	I_F = 1.2A		300		ns
T_{pr}	Forward Recovery Time			200		ns

LOGIC LEVELS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INL}, V_{ENL}	Input LOW Voltage		-0.3		0.8	V
V_{INH}, V_{ENH}	Input HIGH Voltage		2		7	V
I_{INL}, I_{ENL}	Input LOW Current	V_{IN},V_{EN} = L			-10	µA
I_{INH}, I_{ENH}	Input HIGH Current	VIN,V_{EN} = H		30		µA

CIRCUIT DESCRIPTION

L6234 is a triple half bridge designed to drive brushless DC motors.

Each half bridge has 2 power DMOS transistors with $R_{ds}ON$ = 0.3Ω. The 3 half bridges can be controlled independently by means of the 3 inputs IN1, IN2, IN3 and the 3 inputs EN1, EN2, and EN3. An external connection to the 3 common low side DMOS sources is provided to connect a sensing resistor for constant current chopping application.

The driving stage and the logic stage are designed to work from 7V to 52V.

Figure 1: PowerSO-20 Transient Thermal Resistance

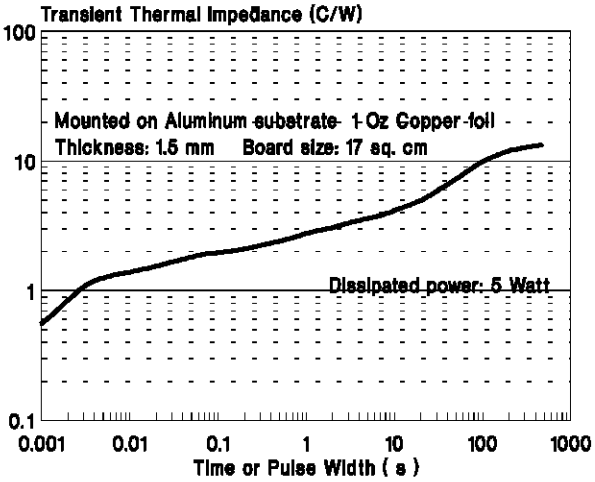


Figure 2: PowerSO-20 Thermal Resistance (Mounted on Aluminium substrate)

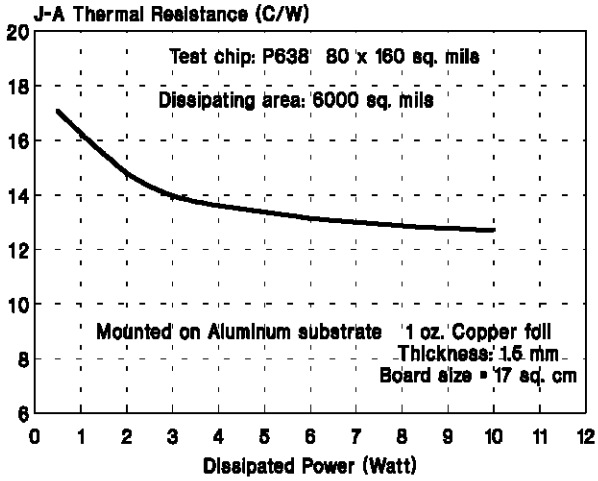


Figure 3: PowerSO-20 Thermal Resistance (Mounted on FR4 monolayer substrate)

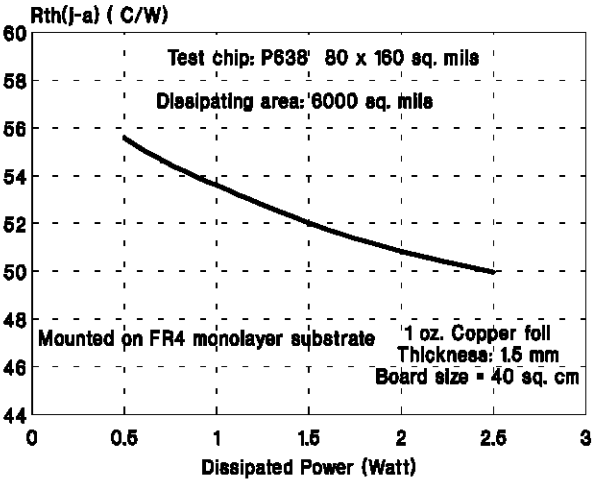


Figure 4: PowerSO-20: with external heatsink

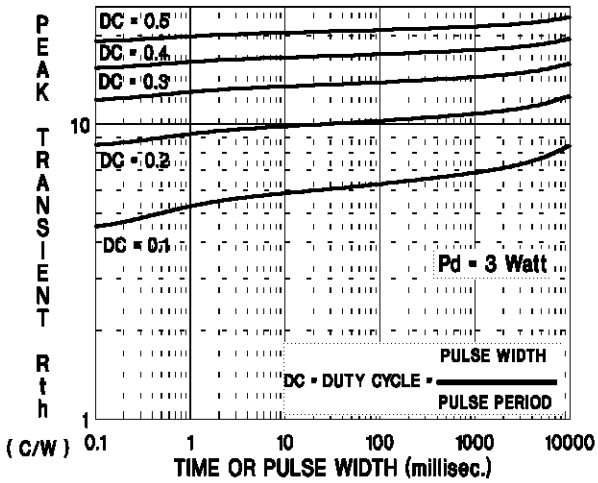
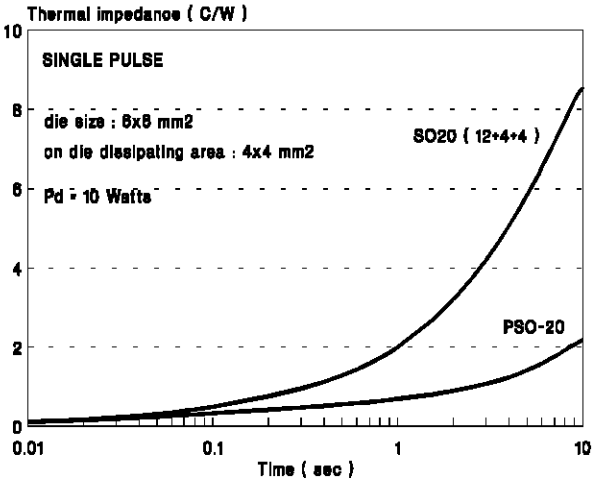


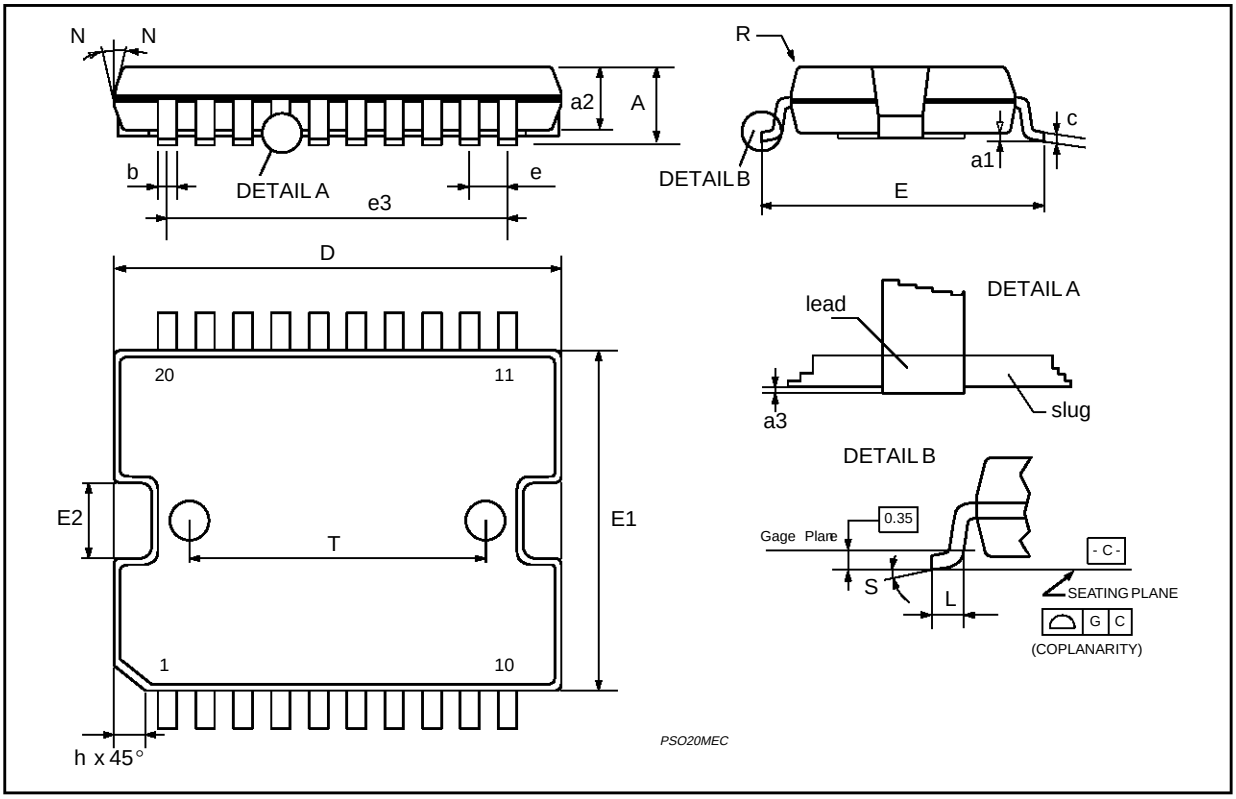
Figure 5: Thermal Impedance of PowerSO-20 and standard SO20



PowerSO-20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.6220		0.6299
E	13.90		14.50	0.5472		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.90		11.10	0.4291		0.437
E2			2.90			0.1141
G	0		0.10	0		0.0039
h			1.10			0.0433
L	0.80		1.10	0.0314		0.0433
N	10° (max.)					
S	8° (max.)					
T		10.0			0.3937	

(1) "D and E1" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (0.006")



POWERDIP 20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050